Fig. 1

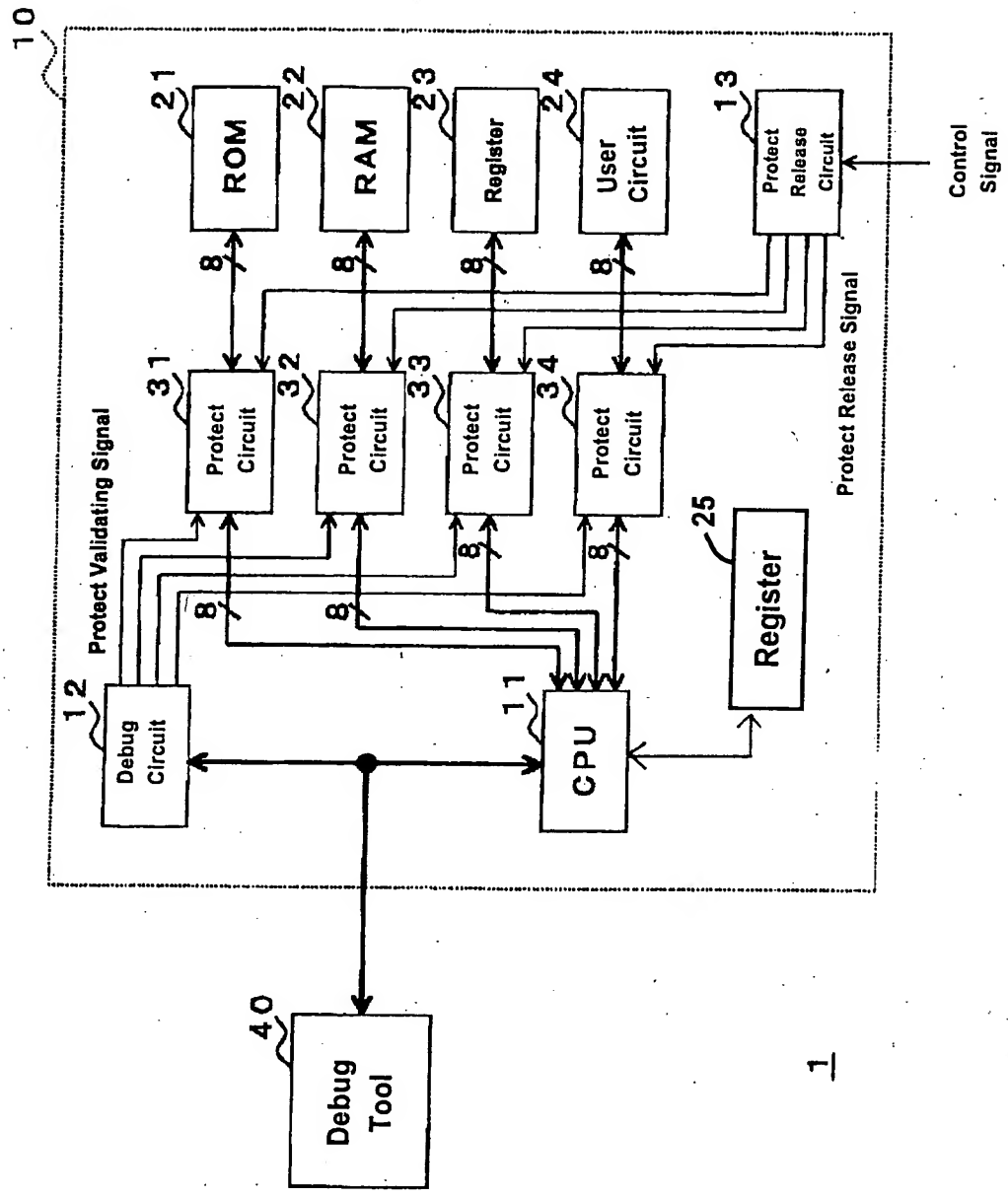

10
21
ROM
22
RAM
23
Register
24
User Circuit
13
Protect Release Circuit
Control Signal
8
31
32
33
34
Protect Circuit
Protect Validating Signal
Protect Release Signal
25
Register
12
Debug Circuit
11
CPU
40
Debug Tool
1

Fig. 2

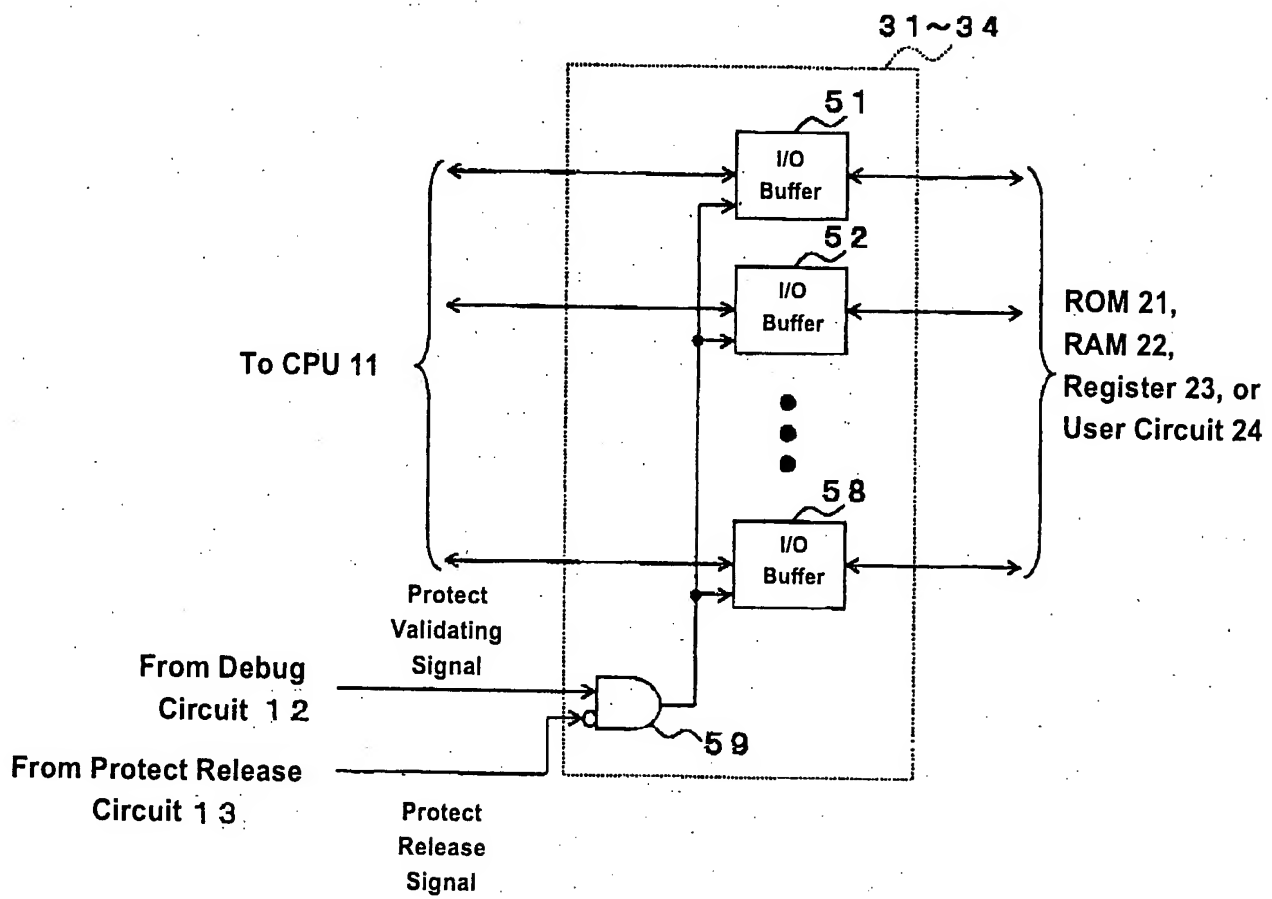

31~34
51
I/O Buffer
52
I/O Buffer
58
I/O Buffer
To CPU 11
ROM 21,
RAM 22,
Register 23, or
User Circuit 24
Protect Validating Signal
From Debug Circuit 12
From Protect Release Circuit 13
59
Protect Release Signal

Fig. 3

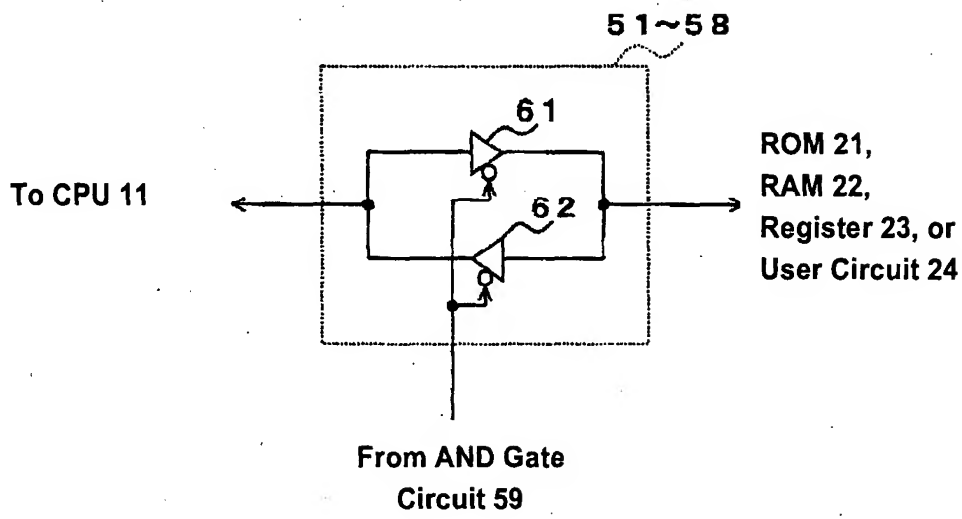

51~58
61
62
To CPU 11
ROM 21,
RAM 22,
Register 23, or
User Circuit 24
From AND Gate
Circuit 59

Fig. 4

Protect Validating Signal	Protect Release Signal	Output of AND Gate Circuit 59	Buffers 61, 62
L	—	L	ON
H	L	H	OFF
H	H	L	ON

Fig. 5

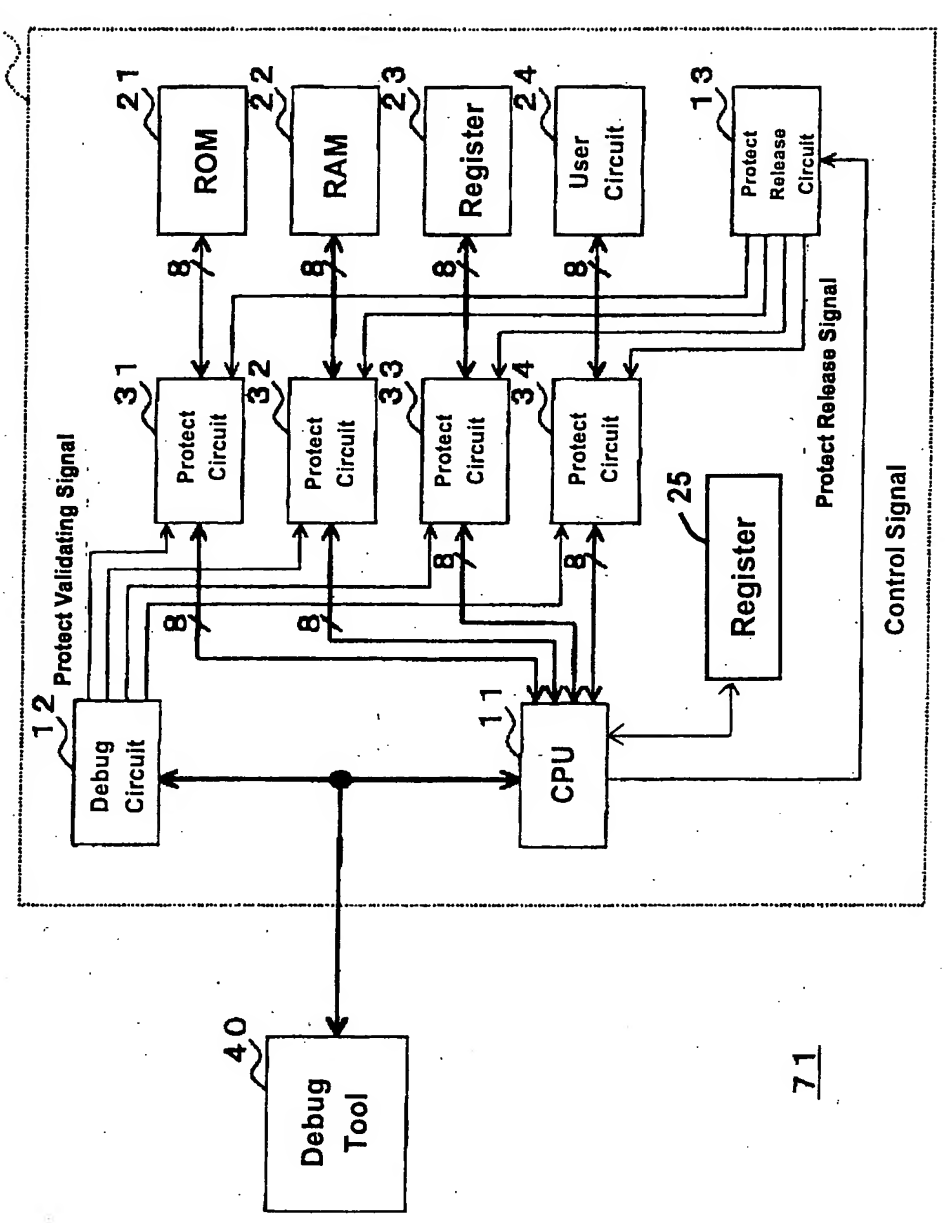

72
ROM
RAM
Register
User Circuit
Protect Release Circuit
21
22
23
24
13
8
Protect Circuit
31
32
33
34
Protect Validating Signal
Protect Release Signal
Control Signal
25
Register
Debug Circuit
12
CPU
11
40
Debug Tool
71

Fig. 6

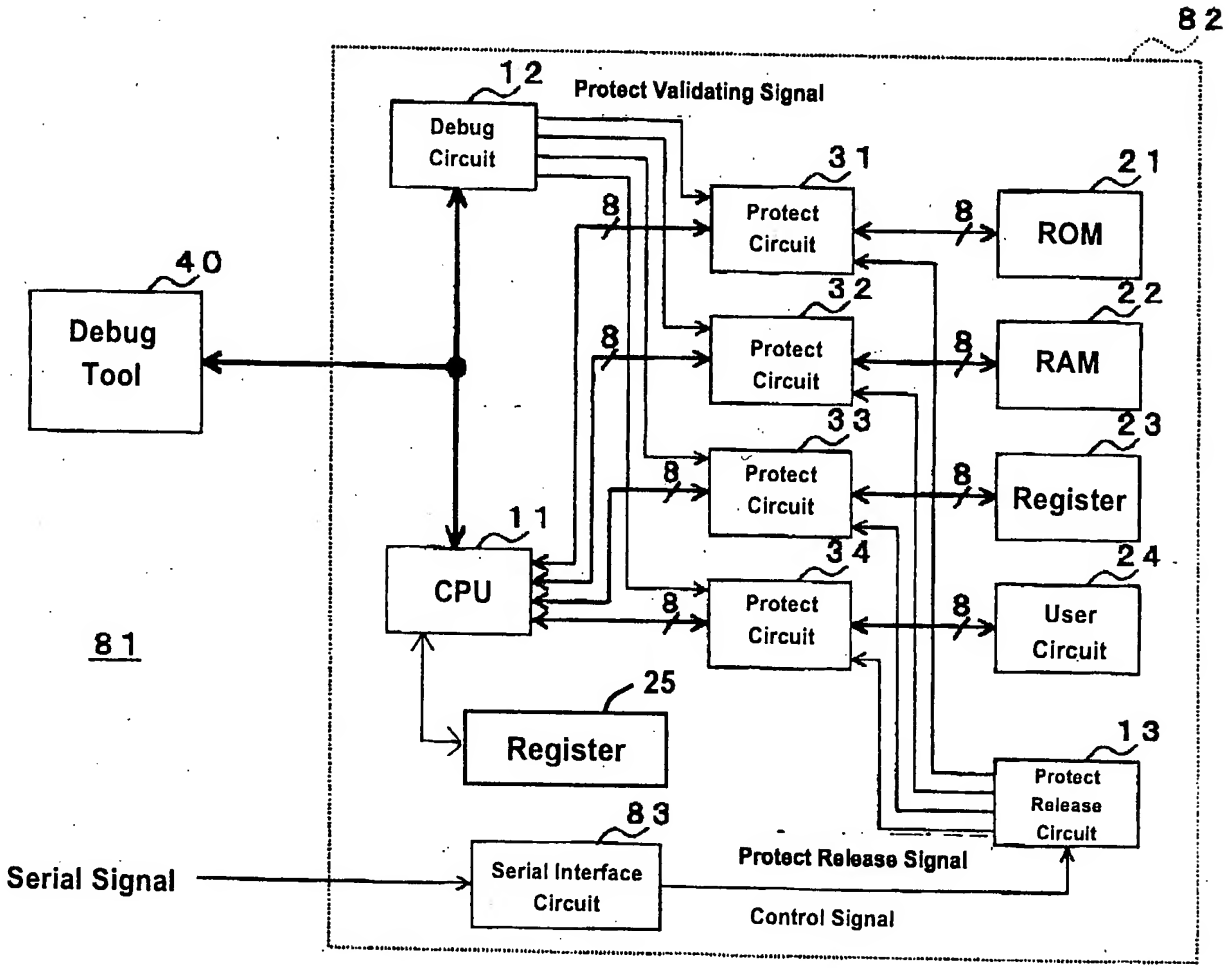

82
12
Protect Validating Signal
Debug Circuit
31
21
Protect Circuit
8
ROM
40
Debug Tool
32
22
Protect Circuit
RAM
33
23
Protect Circuit
Register
11
CPU
34
24
Protect Circuit
User Circuit
81
25
Register
13
Protect Release Circuit
83
Serial Signal
Serial Interface Circuit
Protect Release Signal
Control Signal

Fig. 7

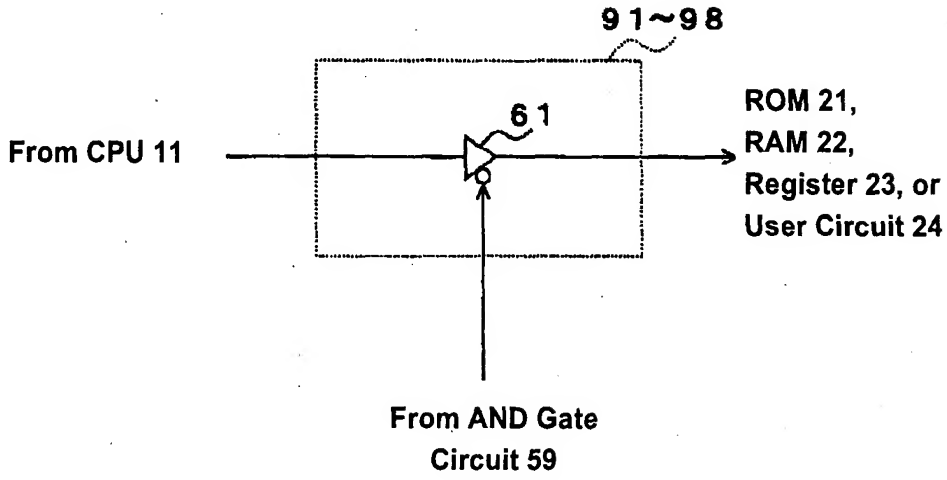

91~98
61
From CPU 11
ROM 21,
RAM 22,
Register 23, or
User Circuit 24
From AND Gate
Circuit 59

Fig. 8

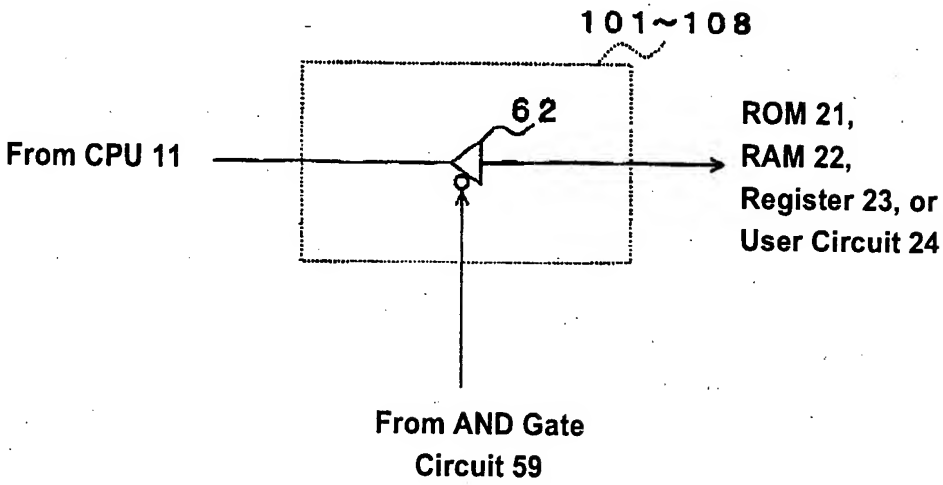
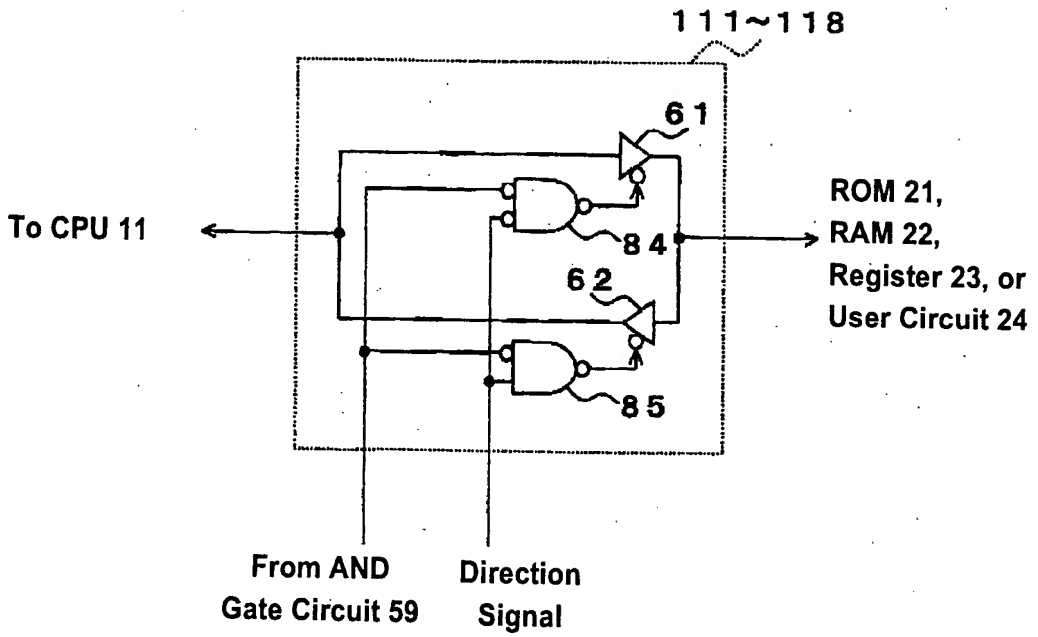

101~108
62
From CPU 11
ROM 21,
RAM 22,
Register 23, or
User Circuit 24
From AND Gate
Circuit 59

Fig. 9


111~118
61
62
84
85
To CPU 11
ROM 21,
RAM 22,
Register 23, or
User Circuit 24
From AND
Gate Circuit 59
Direction
Signal